

What is Claimed is:

1        1. During the testing of the operation of processing  
2 unit, a system for identifying the occurrence of a pause  
3 point condition in the processing unit instruction  
4 execution, the system comprising:

5        timing trace apparatus responsive to signals from the  
6 processor unit, the timing trace apparatus generating a  
7 timing trace stream;

8        program counter trace apparatus responsive to signals  
9 from the processing unit, the program counter trace  
10 apparatus generating a program counter trace stream; and

11        synchronization apparatus applying periodic signals to  
12 the timing trace apparatus and to the program counter trace  
13 apparatus, the periodic signals resulting in periodic sync  
14 markers in the timing trace stream and in the program  
15 counter trace stream.

16        wherein the program counter trace apparatus is  
17 responsive to a pause point signal, the program counter  
18 trace apparatus generating a sync marker signal group  
19 identifying the occurrence of the pause point signal and  
20 relating the pause point signal to the timing trace stream  
21 and to the program code execution.

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23        2. The system as recited in claim 1 wherein the  
24 marker signal group includes a program counter address, a  
25 timing index and a periodic sync ID.

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2       3.   The system as recited in claim 1 further  
3       comprising:

4       data trace apparatus responsive to signals from the  
5   processing unit, the data trace apparatus generating a data  
6   trace stream, wherein the periodic signals are applied to  
7   the data trace apparatus resulting in periodic sync markers  
8   in the data trace stream; and

9       a host processing unit, the host processing unit  
10   responsive to the timing trace stream, the program counter  
11   trace stream and the data trace stream, the host processing  
12   unit reconstructing the processing activity of the  
13   processing unit from the trace streams.

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15       4.   The method for communicating an occurrence of a  
16   pause point in instruction execution of a target processor  
17   unit to a host processing unit, the method comprising:

18       generating a timing trace stream, a program counter  
19   trace stream, and data trace stream, and

20       in the program counter trace stream, including a  
21   program pause point sync marker signal group indicating an  
22   occurrence of a pause point signal and relating the signal  
23   occurrence to the data trace stream and to the timing trace  
24   stream.

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26       5.   The method as recited in claim 4 further  
27   including:

1       including periodic sync markers in the timing trace  
2 stream and in the program counter trace stream; and  
3       including in the pause point sync marker reference to  
4 a periodic sync marker.

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6       6. In a processing unit test environment wherein a  
7 target processor transmits a plurality of trace streams to  
8 a host processing unit, a pause point sync marker signal  
9 group in a trace signal stream, the marker signal group  
10 comprising:

11       indicia of the occurrence of a pause point signal;

12       indicia of the relationship of the occurrence of the  
13 pause point signal to the target processor clock; and

14       indicia of the relationship of the occurrence of the  
15 pause point signal to the target processor program  
16 execution.

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18       7. In a target processing unit generating trace test  
19 signals for transfer to a host processing unit, a program  
20 counter trace generation apparatus comprising:

21       sync marker assembly apparatus, the sync marker  
22 assembly apparatus including:

23           a storage unit;

24           a decoder unit responsive to a pause point signal  
25 for storing an indicia of the pause point signal in the  
26 storage unit, the decoder unit generating a control signal;

1           a gate unit having a timing index, a periodic  
2 sync signal, and a program counter address, the gate unit  
3 storing the timing index, the periodic sync signal and the  
4 program counter address in the storage unit in response to  
5 the control signal; and

6           a FIFO unit, the storage unit transferring the  
7 stored signals to the FIFO unit in the form of a pause  
8 point sync marker.

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10       8. The program counter trace apparatus as recited in  
11 claim 7 responsive to a selected control signal for  
12 transferring the pause point sync marker in the FIFO unit  
13 to an output port of the target processor.

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15       9. The program counter trace apparatus as recited in  
16 claim 8 wherein the apparatus can form a periodic sync  
17 marker in response to a periodic sync signal.

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19       10. The program counter trace apparatus as recited in  
20 claim 9 wherein the pause point signal indicates a  
21 suspension of instruction execution during a change from an  
22 original code sequence to a new code sequence.

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24       11. The program counter trace apparatus as recited in  
25 claim 10 wherein the first instruction code sequence is one  
26 of an original interrupt service routine code or an  
27 original program code and the second instruction sequence

1 is one of a new interrupt service routine and a new program  
2 code.

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